Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Currently Amended) ~~The microcomputer according to claim 1,~~ A microcomputer having an on-chip debugging function, comprising:

a central processing unit for executing instructions; and

a first monitor section which performs data transfer to and from a second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, a monitor program for executing a processing of said first monitor section is stored in a ROM, said second monitor section being provided outside said microcomputer and performing a processing to convert a debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section, and said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

3. (Currently Amended) ~~The microcomputer according to claim 1,~~ A microcomputer having an on-chip debugging function, comprising:

a central processing unit for executing instructions; and

a first monitor section which performs data transfer to and from a second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, a monitor program for executing a processing of said first monitor

section is stored in a ROM, said second monitor section being provided outside said microcomputer and performing a processing to convert a debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section, and the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

4. (Original) The microcomputer according to claim 2, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on the memory map in the debugging mode.

5. (Currently Amended) ~~The microcomputer according to claim 1,~~ A microcomputer having an on-chip debugging function, comprising:

a central processing unit for executing instructions; and

a first monitor section which performs data transfer to and from a second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, a monitor program for executing a processing of said first monitor section is stored in a ROM, said second monitor section being provided outside said microcomputer and performing a processing to convert a debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section, and the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

6. (Original) The microcomputer according to claim 2, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing

unit are saved, and having an address thereof allocated on the memory map in the debugging mode.

7. (Currently Amended) The microcomputer according to ~~claim 1, further~~ claim 3, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

8. (Original) The microcomputer according to claim 2, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

9. (Currently Amended) The microcomputer according to ~~claim 1, the~~ claim 3, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

10. (Original) The microcomputer according to claim 2, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

11. (Currently Amended) The microcomputer according to ~~claim 1, wherein~~ claim 3, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

12. (Original) The microcomputer according to claim 2, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

13. (Currently Amended) The microcomputer according to ~~claim 1, further~~ claim 3, further comprising a trace section realizing a real-time trace function and connected to said second monitor means.

14. (Canceled)

15. (Currently Amended) The microcomputer according to claim 1, said first monitor section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

16. (Original) The microcomputer according to claim 2, said first monitor section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

17. (Currently Amended) The microcomputer according to ~~claim 1, said~~ claim 3, said first monitor section includes a monitor RAM which is readable and writable, and when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

18. (Original) The microcomputer according to claim 2, said first monitor section includes a monitor RAM which is readable and writable, and when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

19. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to ~~claim 1;~~ claim 3;

an input source of data to be processed by said microcomputer;

and

an output device for outputting data processed by said microcomputer.

20. (Original) An electronic instrument, comprising:

a microcomputer according to claim 2;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

21. (Original) An electronic instrument, comprising:

a microcomputer according to claim 3;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

22. (Original) An electronic instrument, comprising:

a microcomputer according to claim 5;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

23. (Original) An electronic instrument, comprising:

a microcomputer according to claim 7;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

24. (Original) An electronic instrument, comprising:

a microcomputer according to claim 9;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

25. (Original) An electronic instrument, comprising:

a microcomputer according to claim 11;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

26. (Canceled)

27. (Original) An electronic instrument, comprising:

a microcomputer according to claim 15;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

28. (Original) An electronic instrument, comprising:

a microcomputer according to claim 17;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

29. (Canceled)

30. (Currently Amended) ~~The debugging system according to claim 29,~~ A debugging system for a target system including a microcomputer, said debugging system comprising:

a second monitor section which performs processing for converting a debugging command issued by a host system into at least one primitive command; and

a first monitor section which performs data transfer to and from said second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, a monitor program for executing a processing of said first monitor section is stored in a ROM, the second monitor section converts the debugging command into the primitive command in order to reduce the size of the monitor program and a scale of the ROM, and said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

31. (Currently Amended) The debugging system according to ~~claim 29, the~~ claim 30, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

32. (Currently Amended) The debugging system according to ~~claim 29, the~~ claim 30, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

33. (Currently Amended) The debugging system according to ~~claim 29, further~~ claim 30, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said

second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

34. (Currently Amended) The debugging system according to ~~claim 29, the~~ claim 30, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

35. (Currently Amended) The debugging system according to ~~claim 29, wherein~~ claim 30, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

36. (Canceled)

37. (Currently Amended) The debugging system according to ~~claim 29, said~~ claim 30, said first monitor section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

38. (Currently Amended) The microcomputer according to ~~claim 29, further~~ claim 30, further comprising a trace section realizing a real-time trace function and connected to said second monitor means.